What is claimed is:

1. A processing element, comprising:

a system bus interface;

an instruction handler;

an input router and conditioner electrically connected to the system bus interface and the instruction handler;

an ALU electrically connected to the input router and conditioner;

a memory electrically connected to the input router and conditioner; and

an output router electrically connected to the ALU, the memory and the input router and conditioner.

2. The processing element of claim 1 wherein the system bus interface and instruction handler comprise:

a connection to a system bus, wherein the system bus comprises a plurality of address lines and a plurality of data lines;

an address decoder, electrically connected to one or more of the plurality of address lines, for determining whether the processing element is selected by comparing a value contained on the one or more address lines with a decoding value and asserting an enable flag when the processing element is selected;

an instruction register, electrically connected to one or more of the plurality of address lines and one or more of the plurality of data lines, for storing the values contained on the one or more address lines and the one or more data lines when the enable flag is asserted; and

a state machine, electrically connected to the instruction register, for configuring the processing element based on at least one of the stored address value and the stored data value.

3. The processing element of claim 1 wherein the input router and conditioner comprises:

a first input path electrically connected to an output of a first input processing element;

a second input path electrically connected to an output of a second input processing element;

a third input path electrically connected to an output of a third input processing element;

one or more multiplexers for determining a data value and an address/data value; and

circuitry for selectively performing one or more operations on at least one of the data value and the address/data value,

wherein the one or more operations include:

performing a bit shift operation on at least one of the data value and the address/data value,

incrementing at least one of the data value and the address/data value,

decrementing at least one of the data value and the address/data value,

storing at least one of the data value and the address/data value, and

passing through at least one of the data value and the address/data value.

4. The processing element of claim 3 wherein the input router and conditioner further comprises a fourth input path electrically connected to a feedback path.

5. The processing element of claim 3 wherein the input router and conditioner further comprises a fourth input path electrically connected to a system bus.

6. The processing element of claim 3 wherein the one or more multiplexers comprise:

a first multiplexer for determining a first portion of the data value;

a second multiplexer for determining a second portion of the data value;

a third multiplexer for determining a first portion of the address/data value; and

a fourth multiplexer for determining a second portion of the address/data value.

7. The processing element of claim 6 wherein the first portion of the data value and the second portion of the data value are of equal width.

8. The processing element of claim 6 wherein the first portion of the address/data value and the second portion of the address/data value are of equal width.

9. The processing element of claim 3 wherein the first input processing element is located along an x-axis with reference to the processing element, the second input processing element is located along a y-axis with reference to the processing element, and the third input processing element is located in a diagonal direction with reference to the processing element.

10. The processing element of claim 1 wherein the input router and conditioner comprises:

a first input path electrically connected to an output of a first input processing element;

a second input path electrically connected to an output of a second input processing element;

a third input path electrically connected to an output of a third input processing element;

one or more multiplexers for determining a data value, an address/data value, and a carry bit; and

circuitry for selectively performing one or more operations on at least one of the data value and the address/data value and the carry bit,

wherein the one or more operations include:

performing a bit shift operation on at least one of the data value and the address/data value,

incrementing at least one of the data value and the address/data value,

decrementing at least one of the data value and the address/data value,

storing at least one of the data value and the address/data value, and

passing through at least one of the data value and the address/data value.

11. The processing element of claim 10 wherein the one or more multiplexers comprise:

a first multiplexer for determining a first portion of the data value;

a second multiplexer for determining a second portion of the data value;

a third multiplexer for determining a first portion of the address/data value;

a fourth multiplexer for determining a second portion of the address/data value; and

a fifth multiplexer for determining the carry bit.

12. The processing element of claim 1 wherein the output router comprises:

a first output path electrically connected to an input of a first output processing element;

a second output path electrically connected to an input of a second output processing element; and

a third output path electrically connected to an input of a third output processing element.

13. The processing element of claim 12 wherein the output router further comprises a fourth output path electrically connected to a feedback path.

14. The processing element of claim 12 wherein the output router further comprises a fourth output path electrically connected to a system data bus.

15. The processing element of claim 12 wherein the first output processing element is located along an x-axis with reference to the processing element, the second output processing element is located along a y-axis with reference to the processing element, and the third output processing element is located in a diagonal direction with reference to the processing element.

16. A method of configuring a processing element comprising:

providing an address value and a data value to the processing element;

decoding the address value;

determining from the decoded address value whether the processing element is selected;

if the processing element is selected, storing at least a portion of the address value and the data value;

loading the stored address value and the stored data value into a state machine associated with the processing element, and

configuring, by the state machine, the processing element based on the stored address value and the stored data value.

17. The method of claim 16 wherein the configuring step comprises:

enabling one or more components of the processing element; and

determining the routing or one or more multiplexers within the processing element.

18. The method of claim 16 wherein the configuring step further comprises:

storing one or more values, determined by at least one of the stored address value and the stored data value, in a memory.

19. A method of configuring a processing element comprising:

providing an address value to the processing element;

decoding the address value;

determining from the decoded address value whether the processing element is selected;

if the processing element is selected, storing at least a portion of the address value;

loading the stored address value into a state machine, and

configuring, by the state machine, the processing element based on the stored address value.

20. A processing element, comprising:

an input block; and

an output block,

wherein the input block comprises:

a first input path electrically connected to an output of a first input processing element,

a second input path electrically connected to an output of a second input processing element,

a third input path electrically connected to an output of a third input processing element, and

wherein the output block comprises:

a first output path electrically connected to an input of a first output processing element,

a second output path electrically connected to an input of a second output processing element, and

a third output path electrically connected to an input of a third output processing element.

21. The processing element of claim 20 wherein the input block further comprises a fourth input path electrically connected to a feedback path.

22. The processing element of claim 20 wherein the input block further comprises a fourth input path electrically connected to a system bus.

23. The processing element of claim 20 wherein the first input processing element is located along an x-axis with reference to the processing element, the second input processing element is located along a y-axis with reference to the processing element, and the third input processing element is located in a diagonal direction with reference to the processing element.

24. The processing element of claim 20 wherein the output block further comprises a fourth output path electrically connected to a feedback path.

25. The processing element of claim 20 wherein the output block further comprises a fourth output path electrically connected to a system bus.

26. The processing element of claim 18 wherein the first output processing element is located along an x-axis with reference to the processing element, the second output processing element is located along a y-axis with reference to the processing element, and the third output processing element is located in a diagonal direction with reference to the processing element.